Digital Control Buck Converter - Reducing the Impact of Load Change on the Output Voltage

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***Abstract*—Power supply circuits used for example to power a high performance electronics systems and modern processors have to keep the supply system stable despite rapid changes of power consumption. For this reason, the choice of the correct transfer function parameters of digital control system in power stage of the converter is particularly important. The study proposes a method of shaping the transfer function of digital control circuit providing effective suppression the output voltage fluctuations when responding to load changes. The method of choosing the transfer function parameters of digital control circuit is shown on the example of the Buck converter controlled by voltage-mode CCM (*Continuous Conduction Mode*).**

***Keywords*—Buck converter; power supply; CCM, digital control**

I. INTRODUCTION

Buck converters are widely used in various types of electrical equipment supply systems because of its high power efficiency, small size and low weight. An important parameter of such converters is the capability to maintain a constant voltage level on the output despite variations in input voltage or load [1–4]. The following methods may be used to output voltage level stabilization: voltage mode (VCM), current mode (CCM) [5–7] or other methods to control of converter [8–19]. The paper presents modeling of transfer function H_s for the digital control circuit of Buck converter using an analog prototype [20–24]. There are also alternative ways of choosing this transfer function [25–28].

The transfer function H_s of digital control circuit was chosen for Texas Instruments TMDSC2KWRKSHPKIT Development Board, taking into account parameters of the following blocks: converter power stage, voltage divider, anti-aliasing filter, propagation delays caused by implementation of the control algorithm in a TMS320F28xxx processor. Issues related to the resolution of ADC (Analog to Digital Converter) and DPWM (Digital Pulse Width Modulation) [29] are omitted in the paper.

II. THE POWER STAGE OF BUCK CONVERTER

Equivalent Circuits of Buck converter power stage is presented in Fig. 1 [30]. Small signal model was used to describe Buck converter power stage with regard to influence of output conductance variations on output voltage level [30–32]. The advantage of this model is, among other things, to simplify the designation of the transfer function of the control block, because there is no need to use the converter output impedance [32].

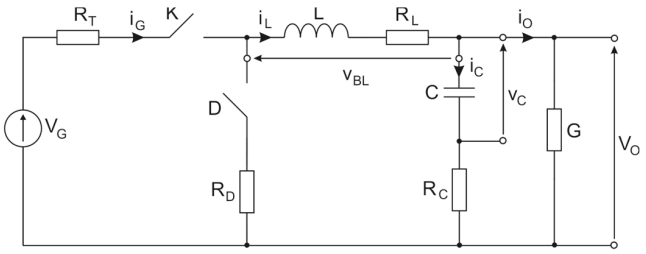

Fig. 1. Equivalent circuits of the power stage of buck converter.

The list of the abbreviations or symbols that are used in the paper:

d_a – small signal component of PWM-signal

v_g – small signal component of PWM-signal

g_t – small signal component of converter load conductance g

v_o – small signal component of output voltage - v_o

H_d – transfer function describing the influences of d_a on v_o

H_g – transfer function describing the influences of g_t on v_o

H_r – transfer function describing the influences of g_t on v_o

The exact description of the use small signal model for shaping the transfer function of analog control circuit of Buck converter is shown in the work [33]. The following coefficients are important:

f_r – resonant frequency of small signal model of power stage of Buck converter, which determines the location of the poles of transfer function H_d in the frequency domain [34–36]

f_{ESR} – The frequency corresponds to the position zero of the transfer function H_d in the frequency domain. Its value is determined by the parasitic capacitance and series resistance of capacitor in the power stage of converter [34–36]

f_{PWM} – Switches in the converter power stage are switched at a constant frequency f_{PWM} . This is the cause of distortion of the control system to which the control system should not respond of PWM-signal [37].

The one of following equation is fulfilled [34]:

$$f_r \ll f_{ESR} < f_{PWM} \tag{1}$$

$$f_r \ll f_{PWM} < f_{ESR} \tag{2}$$

III. VOLTAGE MODE CONTROL

Voltage mode control of buck converter is general method for stabilizing output voltage [34–36]. The advantages of this method are: high effectiveness of output voltage stabilizations and accuracy, and also ease of hardware implementation. Small signal model of Buck converter with voltage mode control is presented in Fig. 2.

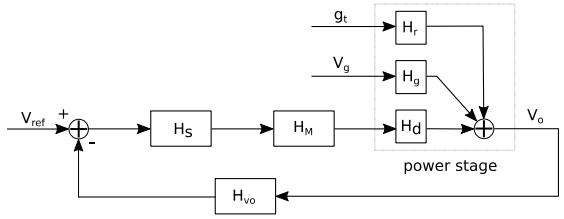

Fig. 2. Small signal model of Buck converter with voltage mode control.

H_s – transfer function of the control block

H_M – transfer function of the digital PWM

H_{vo} – transfer function of the voltage divider, anti-aliasing filter (serial connection)

The small signal model describes the main control block of Buck converter as presented earlier in this paper [30–32]. PWM modulator generates a signal to control power stage of converter. The operating of the PWM modulator is described by the transfer function H_M containing the ideal delay [20, 21, 24, 26, 38, 39]:

$$\mathrm{H_M} = e^{-s \cdot td} \tag{3}$$

where

t_d – total delay introduced by the digital circuit

Desired closed-loop characteristics is achieved by shaping open loop transfer function H_{OL}, using Bode plots. The transfer function H_{OL} is given by the equation:

$$\mathrm{H_{OL}} = \mathrm{H_s} \cdot \mathrm{H_M} \cdot \mathrm{H_d} \cdot \mathrm{H_{vo}} \tag{4}$$

where

H_s – the transfer function of the control circuit

H_M – the transfer function of the PWM

H_d – the transfer control function of the converter power stage

H_{vo} – the transfer function of the voltage divider with anti-aliasing filter

Stabilization of the output voltage is effective if following inequality will be satisfied [35, 36]:

$$|\mathrm{H_{OL}}| \gg 1 \tag{5}$$

Using transfer function H_{OL} to find the transfer function of control circuit H_s it should be considered that inequality (5) can be fulfilled only for frequencies less than ~ 0.5 f_s. Otherwise, the control circuit would be sensitive to the noise generated by the power stage of converter (switching noise). The value of the frequency f_c for which the equation (6) is satisfied should be as large as possible, then the control circuit is more responsive to changes in the output voltage. The method used to evaluate stability and shape of the transfer function H_{OL} of the control circuit are given in the papers [35, 36].

$$|\mathrm{H_{OL}}(f_c)| = 1 \tag{6}$$

IV. SHAPING OF THE TRANSFER FUNCTION H_S OF CONTROL CIRCUIT

Transfer function of control circuit has to maintain the output voltage constant irrespective of v_g and g_t changes. Usually, for practical and economical reasons, and also due to the properties of transfer function H_d of main converter block, preferred embodiment of transfer function having two zeros and three poles, which is referred to as "type III" in the literature [20, 21, 24, 34–36]. The type III has the form:

$$\mathrm{H_{s2z3p}} = K_{dc} \cdot \frac{(s-z_1)\cdot(s-z_2)}{(s-p_1)\cdot(s-p_2)\cdot(s-p_3)} \tag{7}$$

All zeros and poles real of H_{s2z3p} are real. Pole p_1 is always placed at zero. It introduces the function of integration enables a steady state to ensure that v_o is the value v_{ref}. Zero z_1 and z_2 are designed to compensate for the phase shift introduced by the transfer control function poles H_d, and the integral component H_s - pole p_1. The phase changes caused by the poles of the transfer functions. The aim is to satisfied inequality (5) for the largest possible frequency range.

To find the transfer function of control the research should start from a distribution of zeros and poles function H_{s2z3p} in Laplace domain so that they satisfied following equations in the frequency domain:

$$\begin{gathered} f_{p1} = 0 \\ f_{z1} \in \langle 0.6 \cdot f_{LC}, 0.9 \cdot f_{LC} \rangle \\ f_{z2} \in \langle 2 \cdot f_{LC}, 5 \cdot f_{LC} \rangle \\ f_{p2} \cong f_{ESR} \\ f_{p3} \in \langle 0.5 \cdot f_{ESR}, 0.9 \cdot f_{PWM} \rangle \end{gathered} \tag{8}$$

where

f_{px} – the frequency corresponding to the position of the pole p_x

f_{zy} – the frequency corresponding to the position of the zero z_y

The k_{dc} coefficient value of transfer function H_{s2z3p} is chosen so that $|H_{OL}|=1$ for the assumed value of the frequency f_c satisfying the condition of $f_c << f_{PWM}$. If $f_{ESR} > f_{PWM}$ then f_{P3} should be placed in the range $\langle 0.5 \cdot f_{PWM}, 2 \cdot f_{ESR} \rangle$ [34].

To improve the ability to reduce impact v_g and g_t on v_o, according to the authors should be considered properties of functions H_g and H_r.

The modulus value of the function H_r presented in Fig. 3 shows that for decreasing–influence of g_t on v_o is most important to have such a properties of H_{OL}:

- as large as possible maximum $|H_{OL}|$ close to the value f_r
- area under the $|H_{OL}|$ curve should be the greatest for frequency range $< 0.5\, f_r, f_c >$ as possible
- the value of f_c should be as large as possible

This will improve reducing influence of v_g to v_o. Comprehensive explanation this recommendation was presented in [33]. The use of a digital PWM and an anti-aliasing filter makes it necessary to application an extra zero of transfer function of analog prototype, function H_{s3z3p} has 3 zeros and 3 poles. Additional zero of function H_{s3z3p} is designed to compensate for the phase shift which is caused by the use of digital modulator, an anti-aliasing filter, etc. Additional zero should be placed in the frequency range (f_r, f_{PWM}) [27]. In Fig. 4 is presented the transfer function of power stage of Buck converter for analog control circuit, and also transfer function H_{dall} for digital control circuit. Function H_{dall} includes properties of digital modulator and anti-aliasing filter. [21, 39].

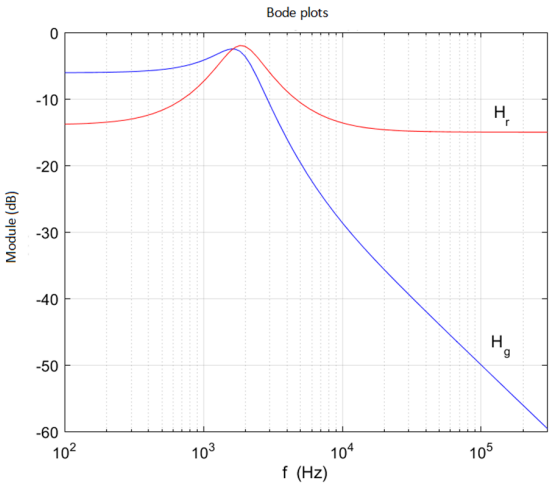

Fig. 3. Bode plots for function H_r and H_g.

The use of Bode plots for transfer function H_{dall} to evaluate stability of the converter and the effectiveness of maintaining the output voltage at a constant level. Accurate information about the changes output voltage v_o due to changes v_g and g_t requires finding the response of the circuit in the time domain. If the changes v_o are too big we should to relocate zeros and poles of the transfer function H_s, once again. If the changes v_o are at an acceptable level than design of function of analog prototype is finished. The transfer function of digital control circuit is obtained by transformation (bilinear, matched) of transfer function H_s of analog circuit.

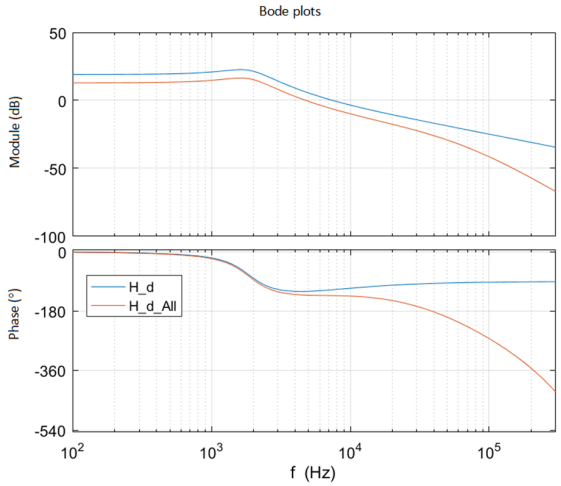

Fig. 4. The transfer functions H_d of power stage and function Hdall (equivalent H_d for digital control)

V. Modeling and Simulation of Buck Converter

Simulation of the proposed model was performed in MATLAB/SIMULINK and Simscape. The digitally-controlled buck converter – Texas Instruments TMDSC2KWRKSHPKIT Development Board was used to verify the proposed method of finding the transfer function of control circuit.

According to the documentation of the Development Board, it was assumed that equivalent circuit parameters are:

L = 10 µH, R_L = 42.4 mΩ, C = 726 mF, R_C = 40 mΩ, G = 1/7.5 S

R_{K1ON} = 5 mΩ, R_{K2ON} = 1.1 mΩ (drain to source resistance in ON state)

f_s = 300kHz, UG = 9V, DA = 0.5

Design assumptions:

PM = 45°, $fc = 0.1\, f_{PWM}$,

$t_d = 0.5/f_{PWM}$ (the delay introduced by the digital control circuit) [20, 23, 39]

Test signals:

step change in the voltage v_g – 0.35 * UG

step change in the load g_t – ½ S

Effects of zeros and poles locations for analog prototype is shown in the three examples. For all the transfer functions H_s of control circuits, transfer function H_{OL} has the same value of frequency f_c. In order to show the importance of authors' design recommendations in one case transmittance H_{s3z3p} was used instead of transmittance H_{s2z3p}. As a result, it was possible to further increase the maximum value of H_{OL} close to the resonance frequency f_r of the power stage of Buck converter.

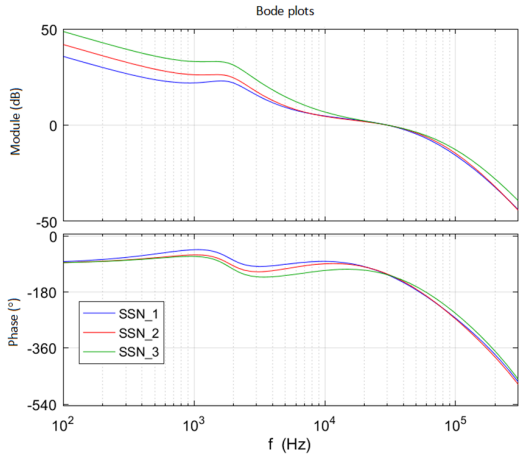

Fig. 5. The transfer functions H_{OL} of analog prototypes H_s

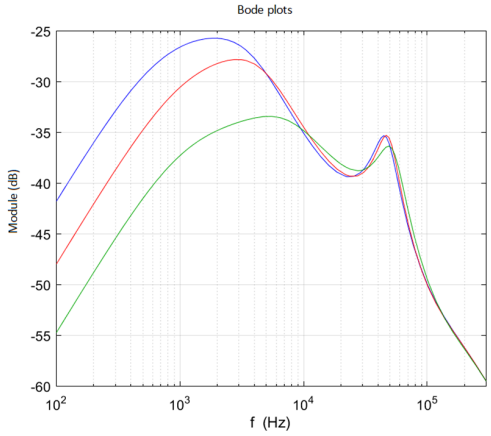

Fig. 6. The transfer function H_{gsz} - attenuation of v_g

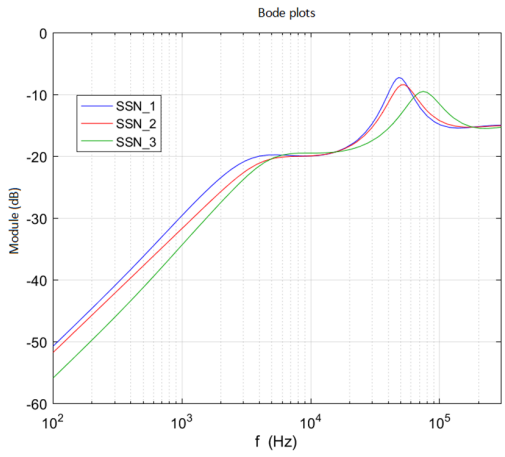

Fig. 7. The transfer function H_{rsz} - attenuation of g_t

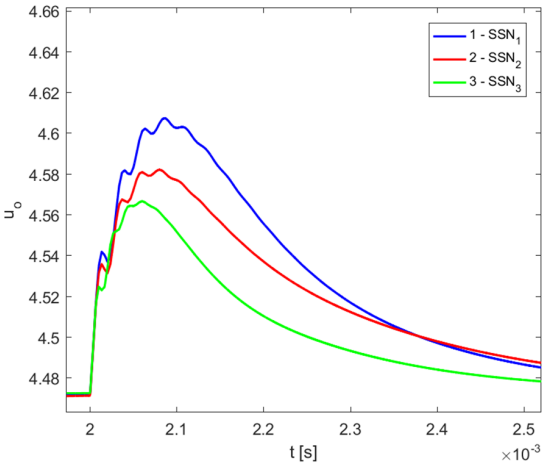

Fig. 8. The response of the converter to a step change of v_g

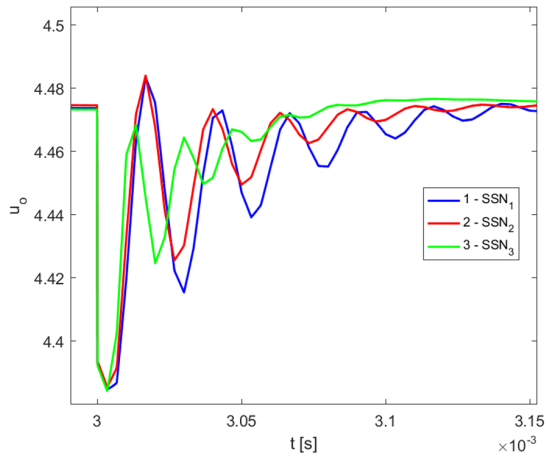

Fig. 9. The response of the converter to a step change of g_t

VI. Concluding Remarks

In the paper authors proposed method of using an analog prototype to find transfer function of digital control block of Buck converter. Presented research confirmed that authors' design recommendations make possible to reduce the influence of changes in the load of the converter on the output voltage. This is confirmed by the Bode plots, Fig. 6, Fig. 7 and time-domain plots Fig. 8, Fig. 9. The method of analog prototype requires taking into account the properties of the digital PWM modulator, an anti-aliasing filter, the divider of output voltage, etc. - Fig. 2. Typically, function type III (H_{s2z3p}) is used to design the transfer function of analog prototype of control circuit. As shown in the examples of design using the function containing one zero more (H_{s3z3p}) allows to suppress influence of changes in supply voltage v_g and load of converter g_t on change the output voltage v_o.

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