

Prototyping of WTA ANNs Using FPAA Devices

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Abstract—A rapid prototyping method for designing a winner takes all (WTA) artificial neural networks (ANNs) has been presented in the paper. The method is based on implementation of field programmable analog arrays (FPAAs) to design WTA ANNs. Programmable synaptic weight connection circuit and 2-WTA circuit are proposed. The 2-WTA circuits are used to configure 4-WTA and 8-WTA circuits. 4-WTA and 8-WTA circuits and programmable synaptic weight connection circuit have been implemented in FPAA device, simulated with a help of the Matlab software and finally measured. Measured characteristics have been compared to simulated ones.

Keywords—artificial neural network; winner takes all circuit; FPAA

I. INTRODUCTION

Recently, rapid advances in VLSI technology has made possible to fabricate mixed (digital and analog) circuits on a single chip. Due to the advances, a design and a manufacturing of mixed circuits become very attractive. Unfortunately, the design of mixed circuits is difficult and time consuming and possible design errors make the design and manufacturing processes emerge as a cost effective. To decrease these costs, reprogrammable devices are commonly used as a fast prototyping tool, before the IC chip is designed and fabricated. Field programmable gate array (FPGA) devices are commonly used as fast prototyping digital systems, and field programmable analog array (FPAA) devices used as fast prototyping analog systems, respectively. The FPGA and FPAA devices provide with several advantages to build hardware systems [1–5] i.e. programmability, parallel processing and of course prototyping. Prototyping with FPGA and FPAA devices allows to overwhelm cost effective manufacturing of the mixed signal circuits. In the paper a winner takes all (WTA) artificial neural network (ANN) has been prototyped with a help of FPAA. The WTA ANN [6–13] is one of the basic structures in ANN systems and provides with efficient solutions for practical applications in analog parallel signal processing (e.g. vector quantization, pattern classification). For prototyping WTA ANN the FPAA device AN221E04 based on switched capacitor technology has been used. The basic WTA building blocks such as: 4-WTA, 8-WTA and programmable synaptic weight circuits, have been designed, implemented in FPAA, simulated and measured.

II. PROPOSED APPROACH

Our prototyping method relies on an analysis of measured parameters of WTA ANN implemented in FPAA device. The network has been tested to verify hardware solution of the ANN.

A. WTA neural network formulation

The WTA network consists of m neurons with programmable synapse weights circuits and WTA circuit as shown in Fig. 1.

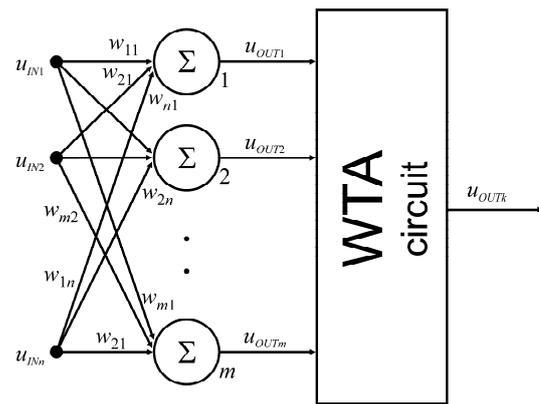


Fig. 1. WTA neural network.

In the WTA network the weight vectors are represented by

$$\mathbf{W}_i = \{w_{i1}, w_{i2}, \dots, w_{in}\} \quad (1)$$

the input voltage vector is represented by

$$\mathbf{U}_{IN} = \{u_{IN1}, u_{IN2}, \dots, u_{INn}\} \quad (2)$$

and the output voltage vector

$$\mathbf{U}_{OUT} = \{u_{OUT1}, u_{OUT2}, \dots, u_{OUTm}\} \quad (3)$$

where n denotes number of input signals, m denotes number of neurons and

$$u_{OUTi} = \mathbf{W}_i^T \mathbf{U}_{IN} = \sum_{j=1}^n w_{ij} u_{INj} \quad i = 1, 2, \dots, m \quad (4)$$

is defined. The WTA function relies on identifying the largest among components of \mathbf{U}_{OUT} . The m^{th} output voltage winner selection, denoted by the index k , is based on the following criterion of maximum activation among all m neurons participating in a competition

$$u_{OUTk} = \mathbf{W}_k^T \mathbf{U}_{IN} = \max_{i=1,2,\dots,m} (\mathbf{W}_i^T \mathbf{U}_{IN}) = \max_{i=1,2,\dots,m} \sum_{j=1}^n w_{ij} u_{INj} \quad (5)$$

B. WTA circuits structures

The m -WTA circuits are composed of identical 2-WTA circuits. The 2-WTA circuit shown in Fig. 2, identifies the smaller of its two voltages and produces an output voltage which is a copy of its local winner.

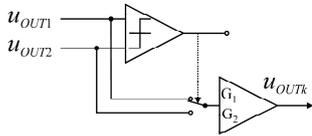


Fig. 2. 2-WTA circuit.

The 4-WTA and 8-WTA circuits, configured from 2-WTA circuits, are shown in Figs. 3 and 4.

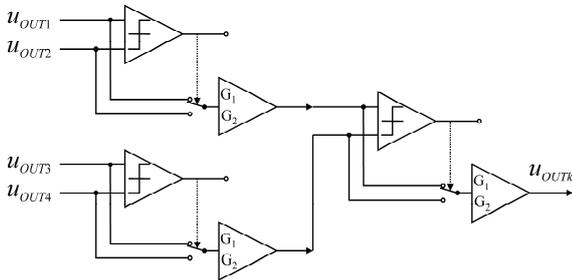


Fig. 3. 4-WTA circuit structure.

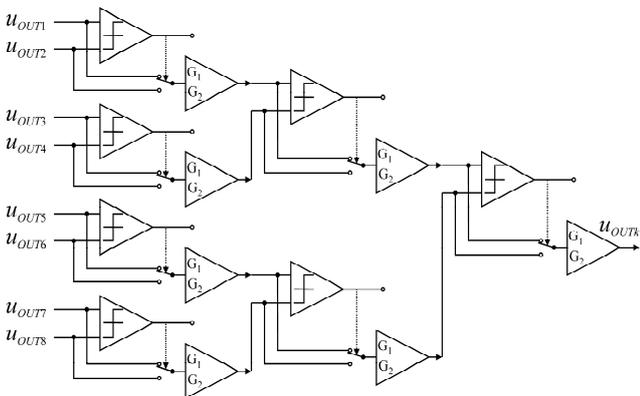


Fig. 4. 8-WTA circuit structure.

C. Programmable synaptic weight circuit structure

Programmability [14–15] is an important feature of WTA ANN. Main problem is to make weights representing synaptic connections that are continuously adjustable, preferably by an analog control signal. The adjustable weight must respond to a learning signal due to the unsupervised training rule it implements. WTA networks competitive learn by moving the weight vector of the winning neuron a fraction of the way, in each update, closer to the input vector. The final result after a finite-training period is that the connection weights approximate the density of the input pattern vectors presented.

Weights of the winning neuron with the largest u_{OUTk} are adjusted, while the weights of the others remain unaffected. As such, WTA basic competitive learning rule to update synaptic weight of the k^{th} neuron that won the competition can be expressed as

$$\mathbf{W}_k^{\text{new}} = \mathbf{W}_k^{\text{old}} + \alpha(\mathbf{U}_{IN} - \mathbf{W}_k^{\text{old}}) \quad (6)$$

where $\alpha > 0$ is a small learning constant. The losing neurons are not allowed to change its weights. Equation (6) can be rearranged to update each vector element (synaptic weights of the k^{th} winning neuron) as follows

$$w_{kj}^{\text{new}} = (1 - \alpha)w_{kj}^{\text{old}} + \alpha u_{INj} \quad (7)$$

Programmability of synaptic weight w_{kj} with respect to learning signal u_{skj} is usually the following linear function

$$w_{kj}^{\text{new}} = f(u_{skj}) = c u_{skj} \quad (8)$$

where c is constant. Taking equation (8) into account in equation (7) the following update for learning signal can be obtained

$$u_{skj}^{\text{new}} = (1 - \alpha)u_{skj}^{\text{old}} + \frac{\alpha}{c} u_{INj} \quad (9)$$

The learning signal is obtained in a structure composed of summer, delay circuit and amplifiers where appropriate gains are equal $1-\alpha$ and α/c . The programmable synaptic weight circuit is shown in Fig. 5.

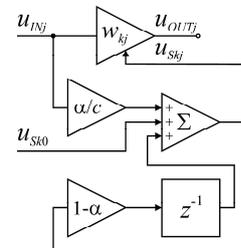


Fig. 5. Programmability of a synaptic weight circuit structure w_{kj} .

III. MATLAB SIMULATION OF WTA STRUCTURES

The WTA ANNs structures have been implemented in four FPAA's of the AN231E04 device. The first step of prototyping competitive WTA ANN with a help of FPAA relies on simulation of 4-WTA and 8-WTA circuit and programmable weight synaptic circuits.

The structures of the 4-WTA and the-8 WTA circuits are implemented in FPAA1 and in FPAA1, FPAA2 and FPAA3, respectively. Their structures and Matlab simulated responses on four and eight signal excitations are shown in Figs, 6 and 7, respectively.

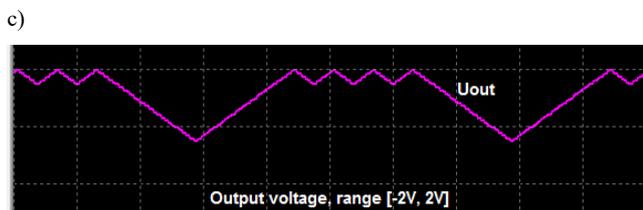
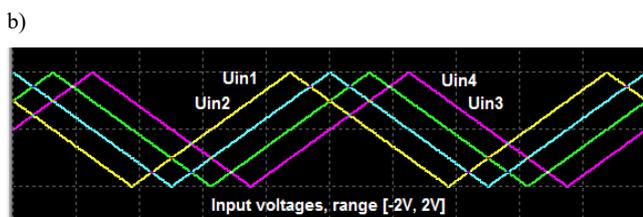
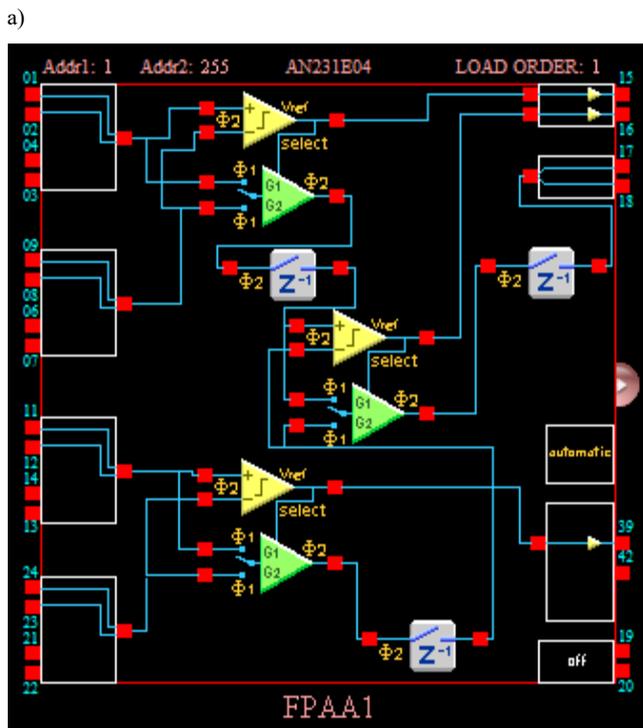


Fig. 6. 4-WTA circuit, a) structure, b) four input excitations, c) response.

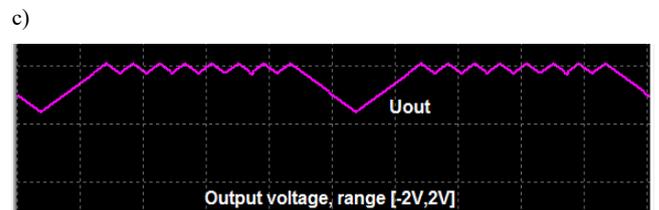
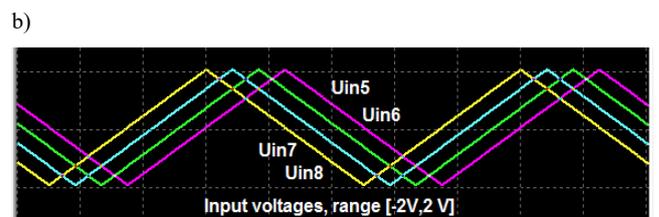
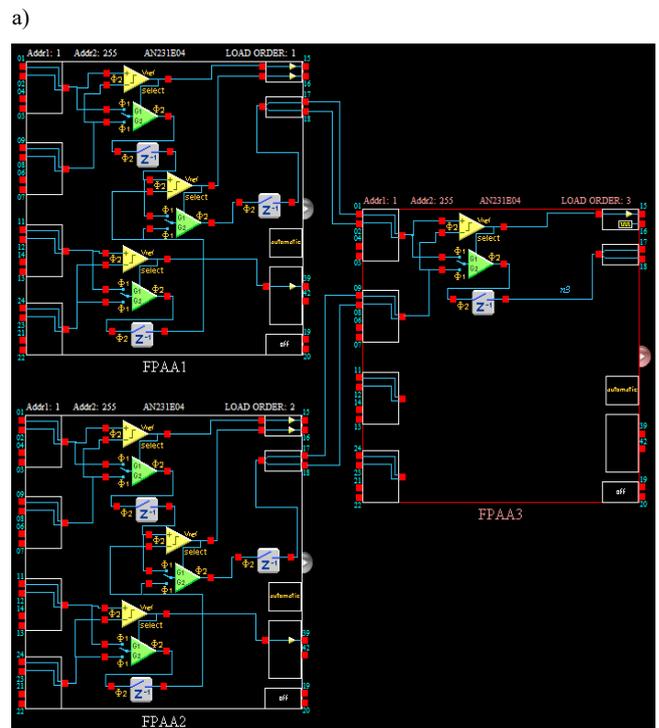


Fig. 7. 8-WTA circuit, a) structure, b) four of eight input excitations, c) response.

The structure of the single programmable synaptic weight circuit structure w_{kj} , described by the equation (8), is implemented in FPAA1. Its structure and Matlab simulated input output transient characteristic is shown in Fig. 8.

IV. EXPERIMENTAL RESULTS

To verify simulation results, the characteristics of FPAA implemented: 4-WTA, 8-WTA and programmable synaptic weight circuits, have been measured. The measured structures and responses of 4-WTA, 8-WTA on four and eight signal excitations are shown in Figs. 9 and 10, respectively.

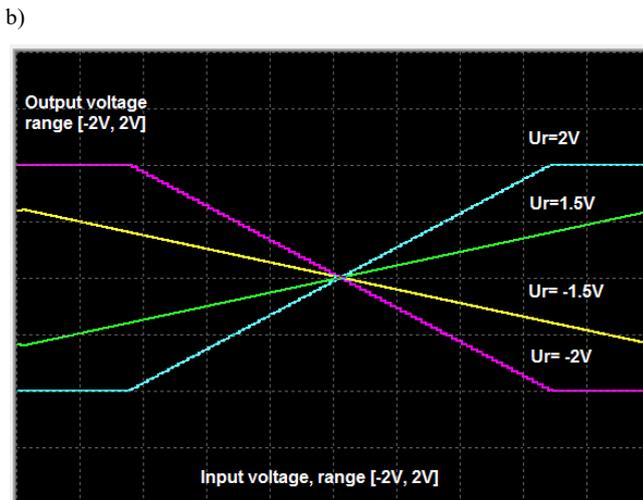
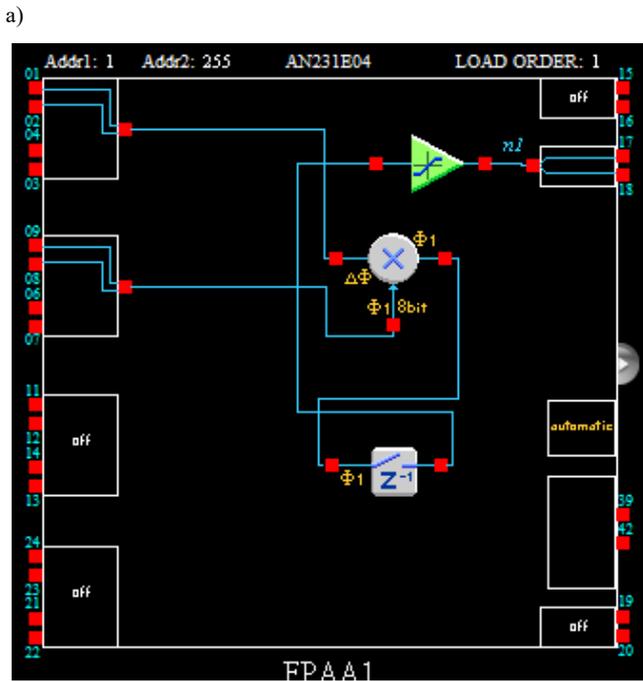


Fig. 8. programmable synaptic weight circuit structure w_{kj} , a) structure, b) input output transient characteristic.

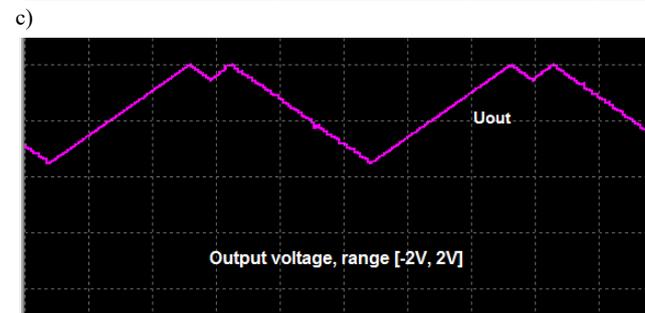
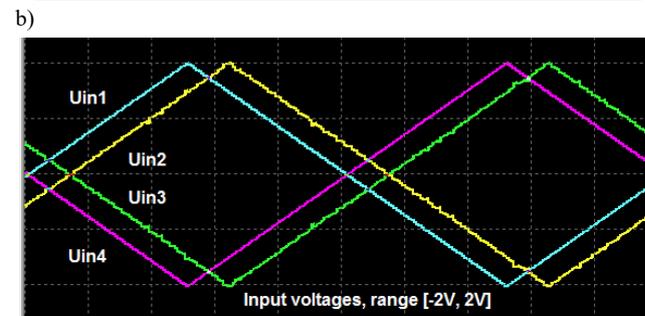
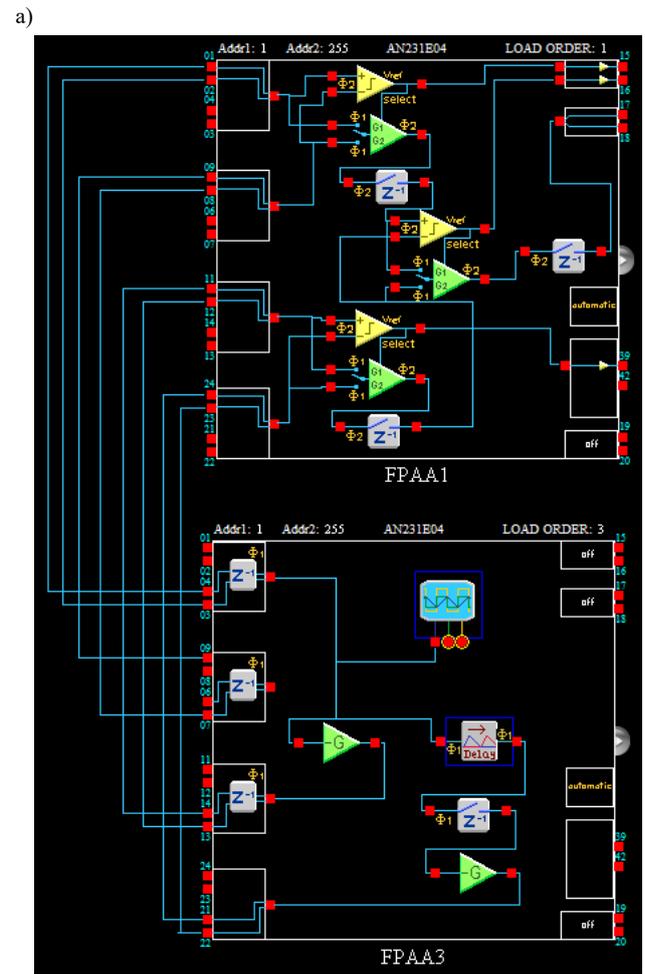


Fig. 9. Measured 4-WTA circuit, a) structure, b) four of eight input excitations, c) response.

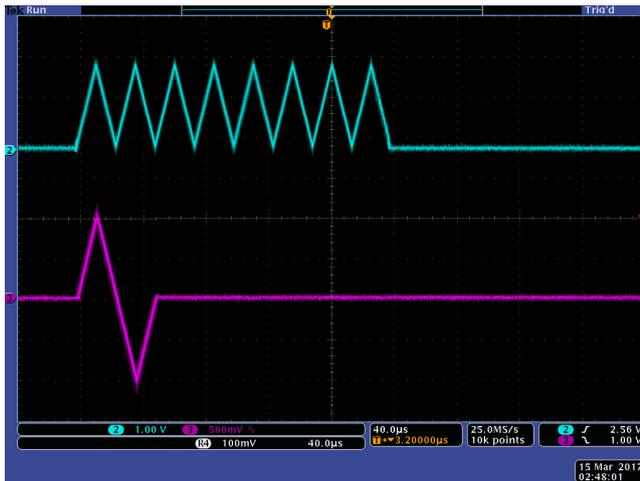


Fig. 10. Measured 8-WTA circuit: response of circuit (upper waveform) and one of eight input excitation (lower waveform). Tektronix MSO 4054

The measured structure of the single programmable synaptic weight circuit structure w_{kj} , described by the equation (8), is implemented in FPAA1 and measured input output transient characteristic are shown in Fig. 11.

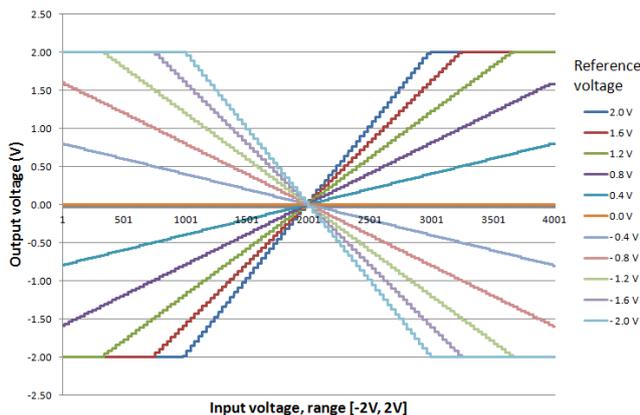


Fig. 11. Measured programmable synaptic weight circuit structure w_{kj} , input output transient characteristic.

It is visible that measured and simulated characteristics of 4-WTA, 8-WTA and programmable weight synaptic circuits are similar, respectively. They confirm that presented WTA circuits offer the potential to prototype competitive WTA ANNs.

V. CONCLUDING REMARKS

Prototyping of WTA ANNs has been presented in the paper. The method is based on implementation of FPAA

AN221E04 to configure and reconfigure proposed circuits. 4-WTA, 8-WTA and programmable synaptic weight circuits have been considered. The circuits characteristics have been simulated and finally measured. Measured performances of the competitive WTA ANNs confirm that FPAA reprogrammable devices such as AN221E04 may be useful for rapid and cost effective prototyping of mixed signal systems.

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